Corrections to the specification

Please replace the paragraph beginning at page 5, line 8, with the following rewritten paragraph:

-- Figures 9A-C illustrate the register maps for the multiprocessor system shown in Figure 1. --

Please replace the paragraph beginning at page 16, line 3, with the following rewritten paragraph:

-- Figure 8 illustrates an example of a preferred embodiment of the bit positions in the registers shown in Figure 7. In particular, for each register in Figure 7, there may be a total of 32 5 bits (bit 0 - bit 31) that may correspond to a particular interrupt source. Some of the bits (bit 14 - bit 31) are not assigned and may be used for later additional interrupts. The assigned bits correspond to interrupts from the USB port/controller, from the universal asynchronous receive/transmit controller (UART A and UART B), from an external source, from the fast USB controller, from the keyboard, from the EIDE controllers (EIDE 1, EIDE 2), from the timers 10 (Timer 1, Timer 2), from the USB reset, from the audio codec (AC 97) and from two other timers (Timer 1 and Timer 2). In this manner, using the VIR and FVIR registers and the above known bit positions, the processors can always determine the source of an interrupt request from the interrupt controller. Figures 9A-C illustrate an example of the actual register maps for the multiprocessor system shown in Figure 1. --